CS8491 COMPUTER ARCHITECTURE

PART – A
(Answer All Questions) 10 x 2 = 20

1. What is an instruction set architecture?
2. How CPU execution time for a program is calculated?
3. How overflow occur in subtraction?
4. What do you mean by subword parallelism?
5. What is a branch prediction buffer?
6. What is instruction level parallelism?
7. What are the various memory technologies?
8. Difference between fine-grained multithreading and coarse-grained multithreading.
9. Point out how DMA can improve I/O speed.
10. How many total bits are required for a direct-mapped cache with 16KB of data and 4-word blocks assuming a 32-bit address?

PART – B
(Answer All Questions) 5 x 13 = 65

11a. (i) What is the need for addressing in a computer system? 3
(ii) Explain the different addressing modes with suitable examples. 10

OR

11b. Explain various instruction formats and illustrate the same with an example. 13

12a. (i) Add the numbers \((0.5)_{10}\) and \((0.4375)_{10}\) using the floating point addition 7
(ii) Multiply the numbers \((0.5)_{10}\) and \((0.4375)_{10}\) using the floating point multiplication 6

OR

12b. Explain in detail about the multiplication algorithm with suitable example and diagram. 13
13a. (i) Explain how the instruction pipeline works?
(ii) What are the various situations where an instruction pipeline can stall? Illustrate with an example

OR

13b. Explain in detail the operation of datapath in MIPS with necessary multiplexer and control lines.

14a. Explain in detail Flynn’s classification of parallel hardware.

OR

14b. (i) What is hardware multithreading?
(ii) Compare and contrast fine grained and coarse grained multithreading

15a. What is virtual memory? Explain in detail about how virtual memory is implemented with neat diagram

OR

15b. (i) Draw the typical diagram of a DMA controller.
(ii) Explain how it is used for direct data transfer between memory and peripherals

PART – C

(Answer All Questions) 15 x 1 = 15

16a. (i) Explain mapping function in cache memory to determine how memory blocks are placed in cache
(ii) Explain in detail about the Bus arbitration techniques in DMA.

OR

16b. A pipeline processor used delayed branch technique. Recommended any one of the following possibility for the design of the processor in the first possibility, the processor has a 4 stage pipeline and one delay slot. In second possibility, it has a 6 stage pipeline and two delay slots. Compare the performance of these two alternatives, taking only the branch penalty into account. Assume that 20% of the instruction are branch instruction and that optimizing compilers has an 80% success rate in filling in the single delay slot, for the second alternative the compiler is able to fill the second slot 25% of the time.